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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Morgan et al.	Docket No.:	TI-25995
Serial No.:	09/088,674	Art Unit:	2674
Filed:	06/02/1998	Examiner:	Nguyen, K.

For: Boundary Dispersion for Mitigating PWM Temporal Contouring Artifacts in Digital Displays

APPEAL BRIEF TRANSMITTAL

May 28, 2002

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner For Patents, Washington, D.C. 20231 on the date below.

Charles A. Brill — 5-28-2002
Charles A. Brill — Date

Transmitted herewith in triplicate is an Appeal Brief in the above-identified application.

Please charge the $320.00 fee for filing the Brief to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Charge any additional fees, or credit overpayment to Deposit Account No. 20-0668. Three copies of this sheet are enclosed.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Morgan et al.	Art Unit:	2674
Serial No.:	09/088,674	Examiner:	Nguyen, K.
Filed:	06/02/98	Docket No.:	TI-25995

For: BOUNDARY DISPERSION FOR MITIGATING PWM TEMPORAL CONTOURING ARTIFACTS IN DIGITAL DISPLAYS

APPEAL BRIEF UNDER 37 C.F.R. § 1.192

May 28, 2002

Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
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Charles A. Brill — 5-28-2002
Charles A. Brill — Date

Dear Sir:

The following Appeal Brief is respectfully submitted, in triplicate, in connection with the above-identified application in response to the Final Rejection mailed November 28, 2001, and the Advisory Action mailed March 13, 2002. Please charge all required fees to deposit account 20-0668.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

This application was originally filed with ten claims, two of which were in independent form. No claims have been allowed. Claims 1-10 are pending and stand rejected.

STATUS OF THE AMENDMENTS

Claims 1 and 6 were amended on October 4, 2000. Responses to rejections were submitted on March 19, 2001, September 10, 2001 without amendments to the claims. A response to the final rejection was submitted on February 19, 2002, but did not propose amendments to the claims.

SUMMARY OF THE INVENTION

Binary spatial light modulators commonly use pulse width modulation (PWM) to generate intermediate intensity levels (specification page 1, line 8 through page 2, line 4). PWM techniques often result in pixels of adjacent intensity levels, or graycodes, having their energy delivered to the pixel at distinctly different times within a frame period (specification page 2, line 5 through page 2, line 21). Large areas of adjacent pixels with intensity codes crossing major PWM bit boundaries—a common situation in natural images—may result in false contours or artifacts in the displayed image (specification page 2, line 22 through page 3, line 11). One embodiment of the present invention eliminates or reduces this artifact by offsetting a pixel by a given positive amount during a first period, and offsetting the pixel by a second amount during a second period (specification page 4, lines 3-5). This technique spreads the major PWM bit boundaries over a region and greatly reduces the resulting image artifacts (specification page 5, lines 5-10). The average pixel value over the two periods, as perceived by the viewer, remains

equal to the nominal pixel value (specification page 4, lines 7-8). A spatial pattern of positive and negative offsets may be used each period to prevent potential image flicker (specification page 4, lines 12-13 and 20-23).

ISSUES

1. Whether Claims 1-10 are unpatentable over U.S. Patent No. 5,995,163 to Fossum ("Fossum") in view of U.S. Patent No. 5,963,261 to Dean ("Dean") under 35 U.S.C. § 103(a).

GROUPING OF THE CLAIMS

Claims 1-10 are independently patentable and stand or fall individually for the reasons more clearly set forth hereinbelow.

ARGUMENTS

Issue 1:

Claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,995,163 to Fossum in view of U.S. Patent No. 5,963,261 to Dean.

With respect to Claim 1, the applicant respectfully submits the Examiner has failed to present a *prima facie* case of obviousness and the rejection should be withdrawn. "A person shall be entitled to a patent unless," creates an initial presumption of patentability in favor of the applicant. 35 U.S.C. § 102. "We think the precise language of 35 U.S.C. § 102 that, "a person shall be entitled to a patent unless," concerning novelty and unobviousness, clearly places a burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103, see Graham and Adams." *In re Warner*, 379 F.2d 1011, 1016 (C.C.P.A. 1967)

(referencing *Graham v. John Deere Co.*, 383 U.S. 1 (1966) and *United States v. Adams*, 383 U.S. 39 (1966)). "As adapted to *ex parte* procedure, *Graham* is interpreted as continuing to place the 'burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103'." *In re Piasecki*, 745 F.2d 1468 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d at 1016).

"The *prima facie* case is a procedural tool which, as used in patent examination (as by courts in general), means not only that the evidence of the prior art would reasonably allow the conclusion the examiner seeks, but also that the prior art compels such a conclusion if the applicant produces no evidence or argument to rebut it." *In re Spada*, 911 F.2d 705, 708 n.3 (Fed. Cir. 1990).

Independent Claim 1 recites, "A method of displaying digital video data comprising pixel values using pulse width modulation, said method comprising the steps of: offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value."

The Examiner has the duty to present a *prima facie* obviousness rejection. Under Graham, this requires determining the differences between the prior art and the claims at issue. The Examiner has utterly failed to read the prior art onto the limitations recited by Claim 1. Without comparison of the prior art to the claim limitations, the Examiner cannot determine the differences between the prior art and the claims at issue. Therefore

the Examiner's statement that "Fossum teaches all of the claimed limitations of claim 1, except for displaying the first offset pixel value during a first display frame, and displaying the second offset pixel value during a second display frame" is unjustified.

The Examiner stated, "Fossum teaches, referring to Fig. 2, a method of digital data which includes a step of positive offsetting 'It+max/2n' at step 206 by a first predetermined amount (+max/2n) to form a first offset pixel value (output $b_{(n-1)2}=1$) and the method of negative offsetting 'It-max/2n' at step 210 by the opposite of the first predetermined amount (-max/2n) to form a second offset pixel value (output $b_n=0$), such that the average of (output $b_{(n-1)2}=1$) and (output $b_n=0$) at step 200 by half scale (min+max)/2 or (0+1)/2 where the lowest (zero scale) value and max is the full scale value (see col. 2, lines 30-32)."

The applicant respectfully submits this statement is not complete. Furthermore, it is a gross mischaracterization of Fossum. Fossum teaches "A digital median filter . . . using a successive approximation A/D converter circuit, which is arranged to produce an output based on majority weighting" (abstract of Fossum).

The Examiner stated, "Fossum teaches, referring to Fig. 2, . . . a step of positive offsetting 'It+max/2n' at step 206 by a first predetermined amount (+max/2n) to form a first offset pixel value (output $b_{(n-1)2}=1$) . . . (see col. 2, lines 30-32)." The passage of Fossum cited by the Examiner states, "The process starts at step 200 by 'guessing' half scale (min+max)/2=0.5 where min is the lowest (zero scale) value and max is the full scale value." The "first offset pixel value (output $b_{(n-1)2}=1$)" referred to by the Examiner merely is one bit of the output digital representation of the median analog value being

generated by Fossum (col. 2, lines 40-43). This cannot be interpreted as "offsetting a first pixel value" as recited by Claim 1.

The Examiner stated, "Fossum teaches, referring to Fig. 2, . . . the method of negative offsetting 'It-max/2n' at step 210 by the opposite of the first predetermined amount (-max/2n) to form a second offset pixel value (output b_n=0) . . . (see col. 2, lines 30-32)." Once again, the "second offset pixel value (output b_n=0)" referred to by the Examiner merely is another bit of the output digital representation of the median analog value being generated by Fossum (col. 2, lines 40-43). Not only can this not be interpreted as "offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value" as recited by Claim 1, it is also completely inaccurate. Since steps 206 and 210 of Fossum are in alternate paths of execution, the value of "n" will change between the time each is executed. Therefore, "-max/2n" is not the opposite of the first predetermined amount "+max/2n" as asserted by the Examiner.

The Examiner stated, "Fossum teaches, referring to Fig. 2, . . . that the average of (output $b_{(n-1)2}$=1) and (output b_n=0) at step 200 by half scale (min+max)/2 or (0+1)/2 where the lowest (zero scale) value and max is the full scale value (see col. 2, lines 30-32)." The applicant will not speculate on what the Examiner intended to mean by this statement, but will point out that, according to Figure 2 of Fossum, the step 200 referred to by the Examiner is executed only once—prior to the offsetting steps 206 and 210 referred to by the Examiner and therefore cannot be construed to compute any sort of average value.

Not only are the teachings of Fossum mischaracterized, the Examiner has also grossly mischaracterized the teachings of Dean. The Examiner stated, "Dean teaches a

related method of displaying the offset pixel value during a the display frame (a progressive scan image and interlaced scan image, see abstract). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include the method of displaying frame taught by Dean in the method of [Fossum's] offsetting pixel data because the usage of 'mid-range' technique (col. 2, lines 61-62 of Dean), any filter (col. 5, lines 53-55 of Dean), combining filter, these are well known techniques (col. 6, lines 1-2 of Dean) which are provided to perform the image quality, to minimize bandwidth, to minimize memory, to implement the 'nearest neighbor' pixels (see col. 3, lines 1-16 of Dean)." The applicant respectfully submits that this, at best, is a conclusory statement and does not address the limitations of Claim 1 or the teachings of either Fossum or Dean. The Examiner has failed to provide any citations of Dean that show, teach, or suggest "displaying said first offset pixel value during a first display frame . . . and displaying said second offset pixel value during a second display frame" as recited by Claim 1.

As stated above, the Examiner has utterly failed to read the prior art of onto the limitations recited by the claims at issue. Without comparison of the prior art to the claim limitations, the Examiner cannot determine the differences between the prior art and the claims at issue and therefore cannot meet the burden of providing a *prima facie* case of obviousness.

The passages cited by the Examiner simply do not support the Examiner's transformation of the teachings of Fossum and Dean to the recited elements of Claim 1, nor is there any basis or suggestion in the prior art to support this novel interpretation of the prior art.

Furthermore, the Examiner has failed to properly combine the teachings of Fossum and Dean. "To support the conclusion that the claimed combination is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed combination or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. & Inter. 1985). The Examiner has not pointed to any teaching in the prior art suggesting the modifications proposed by the Examiner. The Examiner's rejection fails to establish a *prima facie* case of obviousness and is unsupported by the prior art. The rejection therefore should be withdrawn and Claim 1 should be allowed to issue.

Claim 2 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. Not only has the Examiner failed to establish a *prima facie* case of obviousness, as argued above with respect to Claim 1, the Examiner's arguments with respect to Claim 2 are not accurate. The Examiner stated, "Fossum teaches the method of the value of a first predetermined amount (+max/2n) is selected as a function of a first offset pixel value (output $b_{(n-1)2}$=1)." Figure 2 of Fossum clearly shows output $b_{(n-1)}^{2}$=1 is determined after the "first predetermined amount (+max/2n)" is added to the iteration. Furthermore, Claim 2 requires "the value of said first predetermined amount is selected as a function of said first pixel value" not as a function of a first offset pixel value as suggested by the Examiner.

The Examiner has not pointed to any teaching in either Fossum or Dean that fairly suggests "the value of said first predetermined amount is selected as a function of said first pixel value." The Examiner's rejection fails to present a *prima facie* case of

obviousness and is unsupported by the prior art and therefore Claim 2 should be deemed allowable.

Claim 3 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. The Examiner failed to establish a *prima facie* case of obviousness, as argued above with respect to Claim 1. The Examiner's arguments with respect to Claim 3 are irrelevant. The Examiner stated, "Fossum teaches the method of a first offset pixel value (output $b_{(n-1)2}=1$) is greater than [or] less than the positive offsetting 'It+max/2n'." The Examiner has not addressed the actual limitation recited by Claim 3, "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed." The Examiner has not pointed to any teaching in either Fossum or Dean that fairly suggests "wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed." The Examiner's rejection fails to present a *prima facie* case of obviousness and therefore Claim 3 should be deemed allowable.

Claim 4 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. The Examiner failed to establish a *prima facie* case of obviousness, as argued above with respect to Claim 1. The Examiner's arguments with respect to Claim 4 are irrelevant. The Examiner stated, "Dean teaches the method of the pixel value is displayed using a plurality of weighted bit-planes (a progressive scan image at a resolution of 1280x720, an interface scan image at a resolution of 1920x1080 or [vice versa], see abstract)." The applicant respectfully submits Dean does not show, teach, or suggest bit-planes as recited by Claim 4. The Examiner has not addressed the actual

limitation recited by Claim 4, "said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame." The Examiner has not pointed to any teaching in either Fossum or Dean that fairly suggests "pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame." The Examiner's rejection fails to present a *prima facie* case of obviousness and therefore Claim 4 should be deemed allowable.

Claim 5 depends from Claim 1 and should be deemed allowable for that reason and on its own merits. The Examiner failed to establish a *prima facie* case of obviousness, as argued above with respect to Claim 1. The Examiner's arguments with respect to Claim 5 are irrelevant. The Examiner stated, "Dean teaches the method of the progressive-to-interlace and interlace-to-progressive which are mutual." The Examiner has not addressed the actual limitation recited by Claim 5, "said first display frame and said second display frame are consecutive." The Examiner has not pointed to any teaching in either Fossum or Dean that fairly suggests "said first display frame and said second display frame are consecutive." The Examiner's rejection fails to present a *prima facie* case of obviousness and therefore Claim 5 should be deemed allowable.

Claim 6 recites, "A system of displaying digital video data comprising pixel values, comprising: a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and display means displaying said first offset pixel value during a first

display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value." The Examiner has not attempted to read Fossum on the limitations of Claim 6.

With regard to Claim 6 the Examiner stated, "Dean teaches a system of displaying digital video data which includes the equivalent logic circuit offsetting pixel value such as mid range technique (col. 2, lines 61-62), any filter (col. 5, lines 53-55), the I-P technique of 'nearest neighbor,[']according to which the closest pixel vertically from the input field is copied to the output frame (see col. 5, lines 53-61), combining filter according to well known technique (col. 6, lines 1-2). It would have been obvious to a person of ordinary skill in the art at the time of the invention to recognize that Dean discloses any filter application (see col. 5, lines 53-55), the well known technique (see col. 6, lines 1-2), to display the first offset pixel value during a first display frame and displaying the second offset pixel value during a second display frame as claimed."

The applicant respectfully submits that the above assertion by the Examiner is merely conclusory and does not meet the Examiner's burden of presenting a *prima facie* case of obviousness.

With regard to the Examiner's assertion that Dean teaches a mid-range technique, the application respectfully submits this is a gross mischaracterization of Dean. The passage referred to by the Examiner as a "mid-range technique" states, "the quality of the interlace-to-progressive conversion is at least high enough for "mid-range" progressive display systems."

The Examiner's citation of Dean's "nearest neighbor" technique—"according to which the closest pixel vertically from the input field is copied to the output frame"—appears to suggest Dean teaches away from the limitations of Claim 6 which recite "displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame."

For the above reasons, the application respectfully submits the Examiner's rejection of Claim 6 as obvious over Fossum in view of Dean is insufficient in law and in fact and should be reversed.

Claim 7 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. Not only has the Examiner failed to establish a *prima facie* case of obviousness, as argued above with respect to Claim 6, the Examiner's arguments with respect to Claim 7 are not accurate. The Examiner stated, "Fossum teaches a first predetermined amount (+max/2n) is selected by the equivalent logic circuit control (Fig. 4) as a function of a first offset pixel value (output $b_{(n-1)2}$=1)." Figure 2 of Fossum clearly shows output $b_{(n-1)}{}^2$=1 is determined after the "first predetermined amount (+max/2n)" is added to the iteration. Furthermore, Claim 7 requires "the value of said first predetermined amount is selected as a function of said first pixel value" not as a function of a first offset pixel value as suggested by the Examiner.

The Examiner has not pointed to any teaching in either Fossum or Dean that fairly suggests "the value of said first predetermined amount is selected as a function of said first pixel value." The Examiner's rejection fails to present a *prima facie* case of obviousness and is unsupported by the prior art and therefore Claim 7 should be deemed allowable.

Claim 8 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. The Examiner failed to establish a *prima facie* case of obviousness, as argued above with respect to Claim 6. The Examiner's arguments with respect to Claim 8 are irrelevant. The Examiner stated, "Fossum teaches a first offset pixel value (output $b_{(n-1)2}=1$) is greater than [or] less than the positive offsetting 'It+max/2n'." The Examiner has not addressed the actual limitation recited by Claim 8, "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed." The Examiner has not pointed to any teaching in either Fossum or Dean that fairly suggests "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed." The Examiner's rejection fails to present a *prima facie* case of obviousness and therefore Claim 8 should be deemed allowable.

Claim 9 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. The Examiner failed to establish a *prima facie* case of obviousness, as argued above with respect to Claim 6. The Examiner's arguments with respect to Claim 9 are irrelevant. The Examiner stated, "Dean teaches the pixel value is displayed using a plurality of weighted bit-planes (a progressive scan image at a resolution of 1280x720, an interface scan image at a resolution of 1920x1080 or [vice versa], see abstract)." The applicant respectfully submits Dean does not address bit-planes. The Examiner has not addressed the actual limitation recited by Claim 9, "said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame

and said second display frame." The Examiner has not pointed to any teaching in either Fossum or Dean that fairly suggests "pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame." The Examiner's rejection fails to present a *prima facie* case of obviousness and therefore Claim 9 should be deemed allowable.

Claim 10 depends from Claim 6 and should be deemed allowable for that reason and on its own merits. The Examiner failed to establish a *prima facie* case of obviousness, as argued above with respect to Claim 6. The Examiner's arguments with respect to Claim 10 are irrelevant. The Examiner stated, "Dean teaches the progressive-to-interlace and interlace-to-progressive which are mutual." The Examiner has not addressed the actual limitation recited by Claim 10, "said first display frame and said second display frame are consecutive." The Examiner has not pointed to any teaching in either Fossum or Dean that fairly suggests "said first display frame and said second display frame are consecutive." The Examiner's rejection fails to present a *prima facie* case of obviousness and therefore Claim 10 should be deemed allowable.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,995,163 to Fossum in view of U.S. Patent No. 5,963,261 to Dean is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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APPENDIX

1. A method of displaying digital video data comprising pixel values, said method comprising the steps of:

   offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and

   offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

2. The method as specified in Claim 1 wherein the value of said first predetermined amount is selected as a function of said first pixel value.

3. The method as specified in Claim 1 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

4. The method as specified in Claim 1 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

5. The method as specified in Claim 1 wherein said first display frame and said second display frame are consecutive.

6. A system of displaying digital video data comprising pixel values, comprising:

a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and

display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

7. The system as specified in Claim 6 wherein the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value.

8. The system as specified in Claim 6 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

9. The system as specified in Claim 6 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

10. The system as specified in Claim 6 wherein said first display frame and said second display frame are consecutive.